REMARKS

Claim Status

Claims 1-8 were pending in the case and prior to the filing of the RCE, all stand rejected. See Advisory Action of August 10, 2006.

In this amendment, Claims 1-8 are amended and new Claims 9-10 added. This amendment is entitled to entry since it is filed after filing of an RCE.

Claim Rejections

In the last Action which substantively rejected the claims (having a mailing date of April 28, 2006), Claims 1-8 were rejected under 35 U.S.C. §103 as unpatentable over the so-called Applicant admitted prior art in view of Kikuchi et al.

These rejections are traversed.

Claim Amendments

All of the earlier pending claims have been amended but only to improve form and not for reasons of patentability. For instance, Claim 1 has been amended in line 2 to say instead of "for setting" to recite "which sets". The deletion of the first occurrence of "operational modes" is to improve form. The insertion of "other" before "data" is to improve form. Further language has been added to Claim 1 indicating the enforcing circuit is coupled to the memory array. Similar amendments have been made to the other claims, including independent Claim 5.

New Claims 9-10 are well supported by the Specification, see especially page 20, lines 3 and following "...so that when the WP# input signal turns into a low level of "0", the data input from the data input terminal are disabled. As a result, the input of control commands is impossible."

Kikuchi et al.

The key to the rejection in the view of the Examiner appears to be the Kikuchi reference. See the Office Action of April 28, page 4, middle of the page where the Examiner states in pertinent part:

> Kikuchi teaches...a circuit that sets a reading mode in a data protection status where the programming and erasing modes are inhibited from being set in accordance with a control signal for protecting predetermined data, regardless of an input control command, as the data is read from the protect circuit whenever any command is executed.

However, it is respectfully submitted that Kikuchi does not meet the relevant aspect of Claim 1, see Claim 1 as amended final clause, "an operational mode enforcing circuit coupled to the memory array and configured to set the first reading mode regardless of the input control command, in a data protection status..." (emphasis added). This feature in accordance with the present invention affords the advantage as pointed out in the Specification at page 20, lines 3 and following as quoted above that "...the data input from the data input terminal are disabled. As a result, the input of control commands is impossible."

Instead, it is respectfully submitted that Kikuchi practices the prior art approach also set forth in the present Specification at page 8, beginning line 10 "...the writing operation or the erasing operation is inhibited, but the flash memory may be set to the status register reading mode." In other words, it is well known to inhibit writing (programming) and erasing, but that is all. That also appears to be the Kikuchi approach when he sets his writes/erase disable mode, also referred by him as the "protect set" mode. This is his write/erase disable signal PROTECT, see Kikuchi column 9, line 64.

However it is respectfully submitted that Kikuchi does not appear to go beyond that. The Examiner cites Kikuchi column 4, lines 67-68, column 5, lines 1-2, and column 5, lines 26-27 and 37-41, as meeting this aspect of Claim 1, but it is respectfully submitted that those passages disclose no more than the disclosure identified in this application at page 8, beginning line 10.

Perhaps the Examiner is relying upon the Kikuchi Summary beginning line 65 of column 4 which states:

> Accordingly, the object of the present invention is to provide a semiconductor memory device which has the protect function of inhibiting the device from writing and erasing data so that even if an erroneous command is taken in due to power noise or command noise, the command may not stand valid, and which thereby improves the operating margin.

However as pointed out above, in fact Kikuchi only discloses to block the writing or erase functions by disabling them. There is no indication or structure whereby this occurs "regardless of the input control command."

As the present inventors have discovered, a way to carry out a really effective erroneous operation prevention is to set the device in the first read mode, regardless of the input control command, during the write protect function. As pointed out further in new Claim 9 this takes place whereby "data input to the memory device is disabled and input of control commands is prevented." Again, no such feature is shown in Kikuchi. Clearly it is also not described in the so-called admitted prior art either.

Therefore, it is clear that Claim 1 distinguishes over Kikuchi due to this feature ("regardless of the input control command") recited in its final clause, as do dependent Claims 2-4 and new Claim 9.

Moreover, new Claim 9 further distinguishes over Kikuchi because it additionally recites "in the data protection status, data input to the memory device is disabled and input of control commands is prevented." This additional aspect is not shown or even suggested in Kikuchi and thereby Claim 9 additionally distinguishes thereover.

Claim 5 distinguishes over Kikuchi even in conjunction with the admitted prior art for at least the same reasons as pertain to Claim 1. Note that the amendments here to Claim 5 parallel those to Claim 1 and again are not for purpose of patentability but are to improve the form of Claim 5.

Claims 6-8 and Claim 10 dependent upon Claim 5 distinguish over the reference for at least the same reasons as does the base claim. New Claim 10 is additionally allowable for the reasons that pertain to similar Claim 9.

Therefore all pending Claims 1-10 are allowable and allowance is requested.

CONCLUSION

Here all pending claims in this application are believed to be in condition for allowance, and the Examiner is requested to withdraw the previously issued rejection and pass this application to issue. The Examiner is invited to telephone the undersigned if it would expedite prosecution of this case.

In the event the U.S. Patent and Trademark Office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing **Attorney Docket No. 577642000100**.

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Respectfully submitted,

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